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| APPLICATION NO.                | FILING DATE<br>01/18/2000 |       | FIRST NAMED INVENTOR  James John Casto | ATTORNEY DOCKET NO.     | CONFIRMATION NO. |
|--------------------------------|---------------------------|-------|--|-------------------------|------------------|
| 09/484,311                     |                           |       |  | 1001-0087               | 9539             |
| 22120                          | 7590 07                   | /2003 |  |                         |                  |
| ZAGORIN O'BRIEN & GRAHAM LLP   |                           |       | EXAMINER                               |                         |                  |
| 401 W 15TH STREET<br>SUITE 870 |                           |       |  | LEE, EUGENE             |                  |
| AUSTIN, TX 78701               |                           |       |  | ART UNIT                | PAPER NUMBER     |
|                                |                           | -     |  | 2815                    |                  |
|                                |                           |       |  | DATE MAILED: 07/25/2003 |                  |

Please find below and/or attached an Office communication concerning this application or proceeding.

## **Advisory Action**

| Application No. | licant(s)    |
|-----------------|--------------|
| 09/484,311      | CASTO ET AL. |
| Examiner        | Art Unit     |
| Eugene Lee      | 2815         |

-- The MAILING DATE of this communication appears on the cover she t with the correspondence address --

THE REPLY FILED 07 July 2003 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued

| Examination (RCE) in compliance with 37 CFR 1.114.   |    |
|--|----|
| PERIOD FOR REPLY [check either a) or b)]   |    |
| <ul> <li>a) The period for reply expires 3 months from the mailing date of the final rejection.</li> <li>b) The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.         ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).</li> </ul>  |    |
| Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b). | ٦. |
| 1. A Notice of Appeal was filed on Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.   |    |
| 2. The proposed amendment(s) will not be entered because:  |    |
| (a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);   |    |
| (b) ☐ they raise the issue of new matter (see Note below);   |    |
| (c) ☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or   | те |
| (d) they present additional claims without canceling a corresponding number of finally rejected claims. NOTE:  |    |
| 3. Applicant's reply has overcome the following rejection(s):  |    |
| 4. Newly proposed or amended claim(s) would be allowable if submitted in a separate, timely filed amendmen canceling the non-allowable claim(s).   | t  |
| 5.⊠ The a) affidavit, b) exhibit, or c) request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.   |    |
| 6. The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.   |    |
| 7.⊠ For purposes of Appeal, the proposed amendment(s) a)⊠ will not be entered or b)□ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.  |    |
| The status of the claim(s) is (or will be) as follows:   |    |
| Claim(s) allowed:  |    |
| Claim(s) objected to:  |    |
| Claim(s) rejected: <u>2-12,15-25 and 27</u> .  |    |
| Claim(s) withdrawn from consideration:   |    |
| 8. ☐ The proposed drawing correction filed on is a) ☐ approved or b) ☐ disapproved by the Examiner.  |    |
| 9. Note the attached Information Disclosure Statement(s)( PTO-1449) Paper No(s).   |    |
| 10. Other:   |    |
| EDDIE LEE<br>Supervisory patent examiner   |    |

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Continuation of 5. does NOT place the application in condition for allowance because: the Examiner does not agree that Macpherson fails to teach a package having a programmable element. Macpherson teaches a vertical fuse structure for integrated circuits. In column 1, lines 45-50, Macpherson teaches that integrated circuits are programmed into packaged units or after installation onto a circuit board. Therefore, Macpherson does indeed teach an integrated circuit (FIG. 1) that is programmed into packaged units. Regarding Crafts, Crafts teaches polysilicon fuse elements within a semiconductor substrate, the fact that the polysilicon fuse elements are within a semiconductor substrate, constitutes a package. The substrate is carrying the fuse array and altogether the fuse array and semiconductor substrate are a package. Regarding Hamdy, Hamdy teaches (see column 1, lines 20-33) that the anti-fuses are disposed in an integrated circuit and that the integrated circuit is then packaged.